WHAT IS CLAIMED IS:

1. A method comprising:
checking a state of a control bit that specifies whether to assemble an output from multiple virtual tributary (VT1.5/VT2) or tributary unit (TU11/TU12) connections or handle the output as an synchronous transport signal (STS) or administrative unit (AU-3/AU-4) connection; and
switching a predetermined number of entries together based on a state of the control bit.

2. The method of claim 1 wherein the control bit is set by a programmer.

3. The method of claim 1 further comprising
handling the output as an STS connection when the control bit is set.

4. The method of claim 1 further comprising
assembling the output from multiple VT/TU connections when the control bit is not set.

5. The method of claim 1 further comprising
handling the output as an AU-3/AU-4 connection when the control bit is not set.

6. The method of claim 1 further comprising
assembling the output from multiple VT connections when the control bit is set.

7. The method of claim 1 further comprising
storing the control bit in a connection memory.

8. The method of claim 1 further comprising storing the control bit in a register.

9. The method of claim 1 further comprising checking a state of a second control bit.

10. The method of claim 9 wherein the second control bit is associated with independent and concatenated payloads.

11. The method of claim 9 further comprising cross-connecting a second payload with a first payload if the second control bit is set.

12. The method of claim 9 further comprising cross-connecting a second payload with a first payload if the second control bit is not set.

13. The method of claim 9 further comprising storing the second control bit in a connection memory.

14. The method of claim 9 further comprising storing the second control bit in a register.

15. The method of claim 8 further comprising checking the second control bit only if the first control bit is set.

16. A computer program product tangible embodied on a computer readable medium, for provisioning cross-connects in network switching environment comprising instructions for causing a computer to:

check a state of a control bit that specifies whether to assemble an output from multiple virtual tributary/tributary unit (VT/TU) connections or handle the output as an synchronous transport signal (AU-3/AU-4) connection; and

switch a predetermined number of entries together based on a state of the control bit.

17. The computer program product of claim 16 wherein the control bit is set by a programmer.

18. The computer program product of claim 16 further comprising instructions to:

store the control bit in a connection memory.

19. The computer program product of claim 16 further comprising instructions to store the control bit in a register.

20. The computer program product of claim 16 further comprising instructions to:

check a state of a second control bit that is associated with independent and concatenated payloads.

21. The computer program product of claim 16 further comprising instructions to store the second control bit in a connection memory.

22. The computer program product of claim 16 further comprising instructions to store the second control bit in a register.

23. The computer program product of claim 16 further comprising instructions to:

check the second control bit only if the first control bit is set.

24. Apparatus comprising:

a memory including a control bit that specifies whether to assemble an output from multiple virtual tributary (VT) connections or handle the output as an synchronous transport signal (STS) connection;

a circuit to check the state of the control bit; and

control circuitry that uses a second memory to switch a predetermined number of entries together based on a state of the control bit.

25. The apparatus of claim 25 wherein the control circuitry is configured to handle the output as an STS connection when the control bit is set

26. The apparatus of claim 25 wherein the control circuitry is configured to assemble the output from multiple VT connections when the control bit is not set.

27. The apparatus of claim 25 wherein the memory includes a second control bit that specifies whether payloads are independent or concatenated, and the control circuit is configured to switch a predetermined number of payloads together based on a state of the second control bit.